Assignment #4

FPGA Based System Design (Spring 2013)

Electronics Engineering Department

Sub-Campus Chakwal

Write Verilog code (behavior level) and test-benches for the following

1. 4x1 Mux
2. 4 to 16 Decoder
3. D Flip Flop with synchronous and Asynchronous reset
4. 8-bit Register with parallel load
5. ALU with following functionalities
   i. A+B
   ii. A-B
   iii. A+1
   iv. A-1
   v. A AND B
   vi. A OR B
   vii. Not A
   viii. A XOR B
6. Memory having capacity of 64K by 16. Should have read/write operations.